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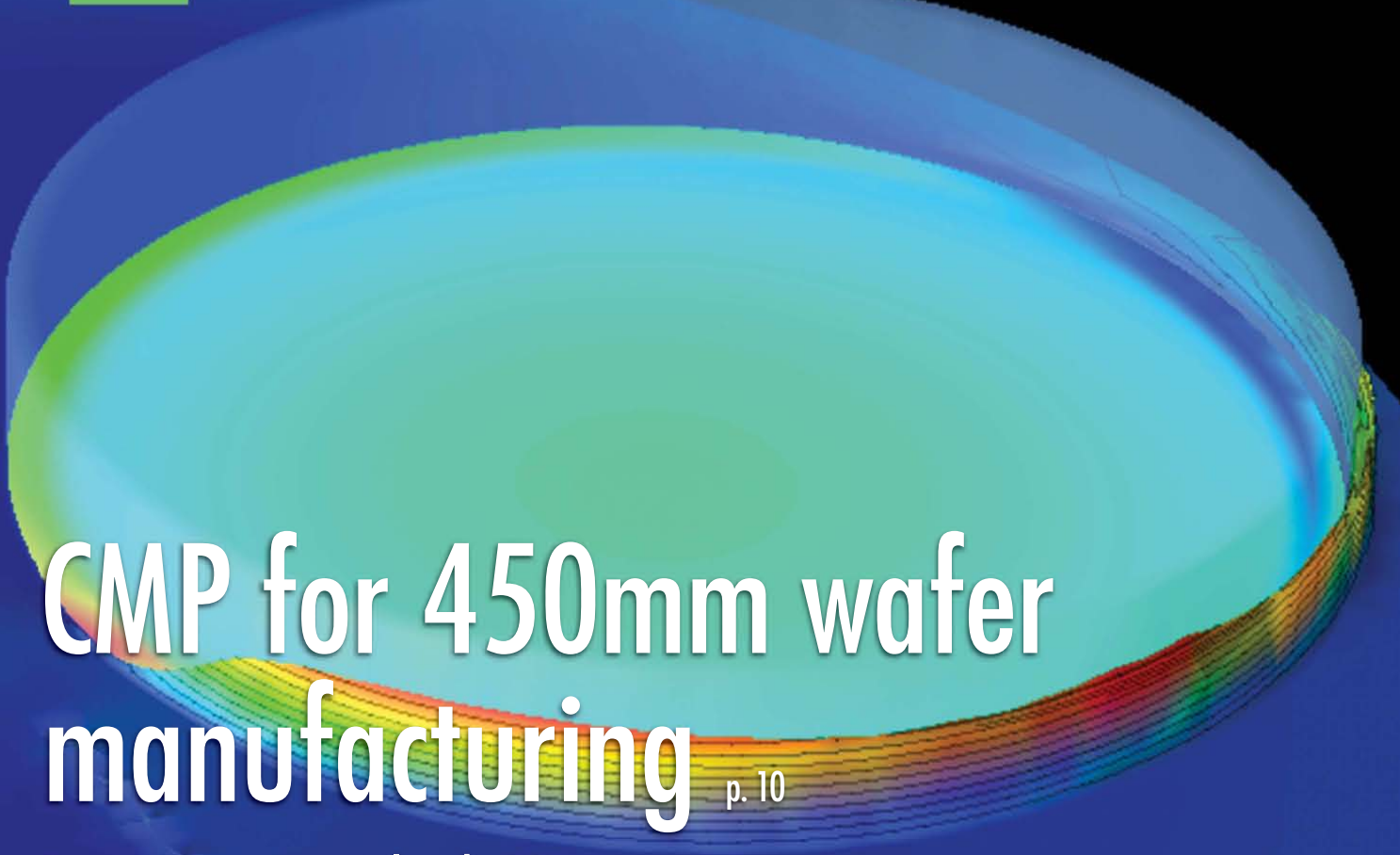
DECEMBER 2009

SolidState TECHNOLOGY

THE INTERNATIONAL MAGAZINE FOR SEMICONDUCTOR MANUFACTURING



CMP for 450mm wafer manufacturing p. 10

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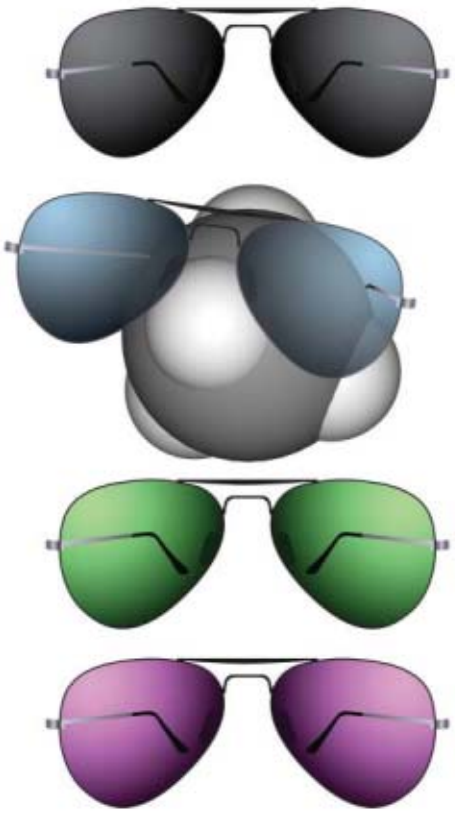

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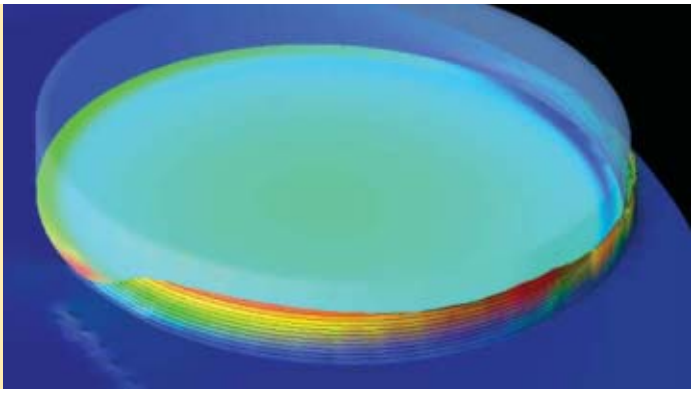

Slurry film thickness on the pad, and the temperature of the wafer and retaining ring for an idealized 450mm CMP tool.

DEPARTMENTS

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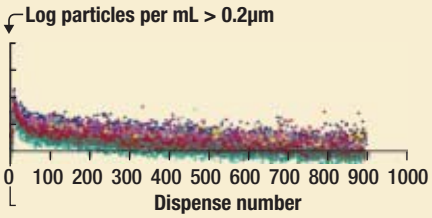
Pressure control for reduced microbubble formation

Microbubbles in leading-edge photoresist materials can distort the exposure pattern and affect yield, sometimes even if proper steps are taken. Entegris' Jennifer Braggin discusses results of a study in which positive pressure applied on the chemistry before the dispense nozzle reduces microbubbles in top anti-reflective coating (TARC).



COO benefits in manufacturing mobile displays with steppers

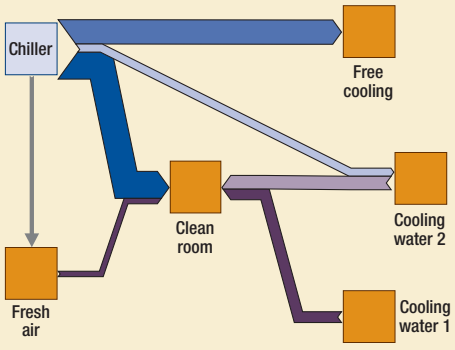
Frank Bok Namgun and Philippe Cochet from Azores discuss the various cost-of-ownership merits of steppers vs. scanners in photolithography for flat-panel displays, including capital equipment and mask costs.

Smooth process development using dispersed teams

A centralized information hub can help overcome the difficulties of process development using a number of dispersed teams, with benefits including faster and more cost-effective development—the importance of which in the current economic climate cannot be underestimated, writes Dirk Ortloff from Process Relations.

Fab support by simulation and scenario comparison

Simple short-cut calculations are difficult for capacity check of facilities in the event of changes in production due to the mutual influence of several facility systems. Only a full software-based calculation model provides enough stability for thorough case studies, according to a trio of experts from M+W Zander.



Single-wafer processing is key to MEMS success

An important lesson for MEMS devicemakers to learn from the semiconductor industry is understanding why single-wafer processing—specifically, dry etching—remains the technique of choice for high-throughput high-yield fabrication, explains memsstar's Tony McKie.

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EDITORIAL

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Facebook, Twitter, LinkedIn, YouTube, Flickr. The use of these and other social networking is exploding, and no one is paying more attention than publishing companies and editors. The prevailing wisdom at press time (it will probably change by the time you read this) is that people are increasingly relying on their social networks for their daily dose of news, and less on traditional print and digital media.

I have personally found LinkedIn to be the best networking site for business, and I have also seen the value in Twitter. Many of the people I follow bring things to my attention that I would not have otherwise seen, with nothing more than a headline and a link. I try to do the same (follow me if you'd like at PetesTweetsPW.com). I, unfortunately, share the same name (no relation) as a Princeton professor who is renowned for his highly controversial views. You can find me on LinkedIn and Facebook by searching "Pete Singer Pennwell."

Facebook for business is a relatively new phenomenon. The big question is whether a high tech industry, such as the semiconductor industry, is ready for it. To that end, I posted a simple question on a popular semiconductor LinkedIn group sites: *"We just started a Facebook page for Solid State Technology. What do you think?* Here's the link if you'd like to become a fan: http://www.facebook.com/pages/Solid-State-Technology/187295754920.

Keeping in mind that this is a LinkedIn group; the responses where overwhelmingly anti-Facebook. "Personally, I try to keep my work and social lives segregated—LinkedIn for work/professional activities and Facebook for non-work/social. I know a few others that attempt to do the same... so, I would vote for LinkedIn groups first," was the first response.

An engineer at Intel followed: "Facebook is useless, unless you want to know that your distant acquaintance had pasta for dinner... Eeeew, gross!" A professor chimed in: "Very bad idea. Not the right place for any discussions on *SST*. Just add a new group here and exclude who you do not want." An analyst piled it on: "Facebook is a waste of time for professional dialog. The Linked In groups are working quite well and geared to the professional people anyway. Twitter is also a waste of time but some people are finding it helpful."

Sensing the pack mentality kicking in, I chimed in with this: "Thanks for the comments. I agree, Facebook has so far been family oriented, with LinkedIn the place for business. But increasingly, businesses and brands are creating Facebook pages, which I think might serve well as a way to informally educate people about the business and recent activities."

One example is Samsung: http://www.facebook.com/fourseasonsofhope.

One group member's response to that was: "It is *quality* not *quantity* of the material that I deem most important for professional users. I now notice the LinkedIn boards (e.g., SPIE) are getting spammed. If one can find a way to differentiate the fluff from the 'true' content, this would be much better: 'informal' versus 'formal/professional.' Otherwise, it becomes a waste of time."

Hmmm. That's what we've been doing with our Web site, magazine and newsletters, but to do that in a social networking environment—without the spam—just might be the trick.

A marketing communications expert (and friend) weighed in with good advice: "Facebook is okay for broad consumer magazines where folks are sharing travel tips and recipes, making it a social tool at best, but not a professional one. I agree with the other comments above. I do use Twitter and like it for business use."

My favorite comment, though, was sent to me privately, I suppose so as not to be cast out by the group: "I just want to share that Facebook may not seem as good or professional networking as Linkedin, but it can be effective to reach your audience, too. Many social media users do not just use only one community for networking. I like your idea! Thanks!"

So, the experiment in social networking begins. We now have Facebook pages for all the brands on ElectroIQ.com, the PennWell Web portal for electronics manufacturing: *Solid State Technology*, *Photovoltaics World*, *Small Times*, *Advanced Packaging* and *SMT*. Scroll down to the bottom and become a fan, if you'd like. Send me suggestions.

Everyone is walking around, eyes on their mobile phone, uploading photos and videos. A new app on the iphone allows you to type while using the built-in camera so that you can actually see where you're going. It's all a great thing for the semiconductor industry in that it can only increase the consumption of electronics and the need for greater bandwidth. Will we see a new blend of business with personal commentary on sites such as Facebook? I think we will. We're all human after all, and humans are social beings. ■

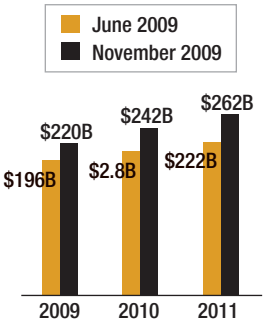
Pete Singer
Editor-in-Chief

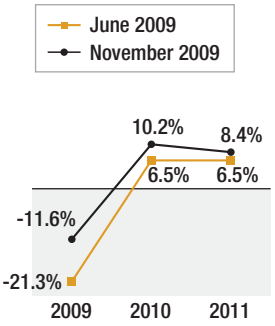
WORLD NEWS

BUSINESS TRENDS

SIA bumps up 2009-2011 forecasts

Betting on the continued impetus of an improving global economy, the Semiconductor Industry Association (SIA) has raised its previous outlook for semiconductor sales over the next three years, with a significantly better view on 2009.





The SIA's previous forecast in June expected a -21% drop in chip sales in 2009 to $195.6B, followed by 6.5% growth in both 2010 (to $208.3B) and 2011 (to $221.9B).

The new forecast has cut the 2009 decline in half, to just an -11.6% decline to $219.7B; 2010 growth is close to double the earlier prognostication, now eking into double-digit growth (10.2%) to $242.1B. And 2011 will be better than expected too, the SIA forecasts, with 8.4% growth to $262.3B.

In a statement, SIA president George Scalise, still emphasizing "cautious optimism," noted that the improved outlooks are closely tied to projections of continued improvement in the worldwide economy. Strong demand for PCs and cell phones (~60% of all semiconductor demand) provide enough confidence in the new marks.

WORLDWIDE HIGHLIGHTS

TSMC has won a US court case against longtime rival **SMIC** of China, taking an 8%-10% ownership stake in lieu of a potentially huge cash payout.

Intel and **Numonyx** say they have built a "vertically integrated" 64Mb test chip enabling stacking of multiple layers of phase-change memory (PCM) arrays within a single die.

Mentor Graphics is launching what it calls a comprehensive test and yield analysis platform incorporating technology homegrown and acquired from **LogicVision**, to help customers drill down through failure analysis data to better identify and fix defects.

SVTC's efforts to offer more leading-edge MEMS technology for its customers now finds it more formally aligned in a new partnership with TSMC.

Rudolph has shipped several backend inspection tools to ASE.

Aeroflex, **Agilent**, and **Test Evolution** are proposing a new modular test standard (AXIe) based on Advanced TCA.

Chartered has adopted **Brion**'s computational lithography technology.

USA

Major changes afoot at the **Semiconductor Industry Association** (SIA): Longtime president George Scalise is retiring in 2010, and the group is uprooting to Washington DC to have "a greater and more effective voice" for semiconductor industry policy concerns.

Applied Materials has acquired the assets of **Advent Solar** in a move to bolster its crystalline silicon (c-Si) technology position against thin-film alternatives (particularly CIGS). Applied also has added copper deposition processing for TFT-LCD manufacturing to its AKT-PiVot 55KV PVD system.

HP has unveiled a new MEMS sensor technology it says is 1000× more sensitive than current products, targeting applications like bridge monitoring.

A new study from **Alchimer** suggests that through-silicon vias (TSV) with higher aspect ratios (20:1 or 10:1, vs. 5:1) offer a significant payback by saving space on a die, exceeding $700 per wafer.

Electroglas has officially reformed its business solely around its wafer prober systems, by selling it to a private financial group formed solely for that purpose, after selling off motion control automation assets to FormFactor.

Specialty TSV foundry **Allvia** is expanding its manufacturing capabilities away from high-cost Silicon Valley to ETEC's former facility in Oregon.

Intersil and **Georgia Tech** have agreed to co-develop high-performance analog chips.

Sanyo has opened a new solar silicon ingot/wafer manufacturing facility in Salem, OR.

Axcelis says a "major foundry" has orderd its Optima XE single-wafer implant tool for high-volume manufacturing of both logic and memory products.

Triquint has received a multiyear $16.2M award from the Defense Advanced Research Projects Agency (DARPA) to explore advanced GaN circuits.

An insider trading scandal has swept up executives at **Intel** and **IBM**, and possibly a former top **AMD** exec as well.

Tegal says it has completed its ProNova ICP process suite rollout for silicon DRIE.

ASIAFOCUS

Spansion Japan plans to sell its 300mm/65nm fab in Aizu-Wakamatsu as part of its bankruptcy reorganization, according to the *Nikkei* daily.

Taiwan's **ProMOS** will make **Elpida**'s 65nm DRAM chips on a foundry basis, modifying most of its tools (total capacity is ~60K WSPM) to be compatible with Elpida processes, notes the *Nikkei* daily. The expected work will amount to 30K-40K WSPM in 2H10, roughly a 20% boost in Elpida's output and putting it in the same ballpark as Samsung and Hynix, the paper said.

Samsung Electronics says it is now focusing its R&D on advanced logic process development for its foundry business, leveraging synergies with its memory development and work with partners and consortia. The chipmaker also has developed what it calls the world's thinnest multi-die package (0.6mm in height), 40% thinner and lighter than current technology.

Hitachi High-Tech is taking over **Renesas**' semiconductor manufacturing tool business.

Korea's **MagnaChip Semiconductor** has emerged from its Chapter 11 bankruptcy filed earlier this year, claiming to be "nearly debt-free" with >$50M cash.

Cree is purchasing a ~600K sq. ft. facility in China's Guangdong Province for its first chip production facility outside North America; the company already has a factory in the area, acquired in 2007.

The **Industrial Technology Research Institute** (ITRI) will add **Applied Materials** to its partners for developing 3D chip stacking technology, by placing "a full line" of AMAT processing tools in its labs.

Flextronics says it will build a new facility in Wuzhong, Suzhou, to support manufacturing and R&D capabilities.

SMIC has adopted **Cadence**'s DFM software for 65nm and 45nm IP/library development and full-chip production.

Carsem has unveiled an "extremely thin" (0.6 × 0.3 × 0.3mm) micro leadframe package (MLP), projecting high-volume offering in early 2010.

EUROFOCUS

IMEC and packaging/assembly firm **Terepac** are collaborating on development of flexible packages for IMEC's biomedical heart monitoring device.

A Norwegian court has agreed to extend **China Sunergy**'s injunction against **REC**, whom it says unjustly terminated a supply deal.

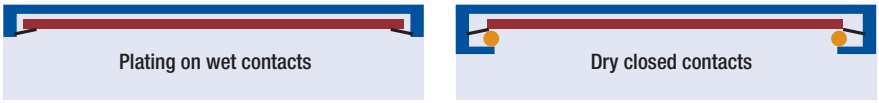
Long-term research, pilot plants, and power producing projects are all key items in a new **European Commission** report on how to support and broaden its solar energy progress and adoption—but Europe's PV industry organization says a stronger push for technology roadmaps and funding are needed as well.

Nova Measuring Systems has booked $2M in metrology tool orders from a memory firm for "first-phase capacity expansion. ■

TECHNOLOGY NEWS

Targeting 22nm and beyond copper electroplating

Novellus Systems recently introduced its Sabre Excel, an advanced copper electroplating system designed to provide fill and defect density performance for the 22nm technology node and beyond. The new technology builds upon the company's Sabre platform.



Comparison of traditional "wet" contact (l) vs. Novellus' dry, sealed contact (r). Plating on contacts can cause defects at small edge exclusion; eliminating plating closes contacts, enabling 1mm edge exclusion process. (Source: Novellus Systems)

To address device reliability concerns associated with copper electroplating at the 22nm node, the industry is trending towards the use of very thin alloy PVD seed layers, explains Sesha Varadarajan, VP & GM of Novellus' electrofill business unit. While thicker PVD seed layers can cause copper voiding, thinner seed layers result in increased seed resistance, making it difficult to achieve the uniform current density required for consistent feature fill during the initial stages of electrochemical deposition (ECD).

According to Varadarajan, the company's new IRISCell technology eliminates this issue by employing patented field shaping elements that enable dynamic current modulation during the deposition process. To ensure a uniform fill process, the electrons have to be distributed equally because the fill process is so sensitive to the current density. "We invented a cell that has focusing elements to distribute the current uniformly preventing edge bias that can narrow, or sometimes eliminate, the window you might have in which a good fill can happen," Varadarajan says.

Thin PVD seeds also create a challenge for uniform nucleation of the copper film. To address this problem, Novellus developed a new "Multiwave" plating process that provides millisecond control of the voltage profile during the initial stages of copper deposition. Millisecond control is "old hat" for vacuum processes, Varadarajan acknowledges, but for plating, it is a leading-edge technology. "Many factors affect the filling process, including absorption and desorption of plating additives from the wafer surface"—proprietary additives in the electrolyte solution that modulate how the fill happens at various points on the wafer, says Varadarajan. "These additives have a time constant associated with absorption/desorption, so there is no benefit to having voltage control that exceeds the time it takes for the additive to come into play. So, millisecond control represents state-of-the-art."

Controlling the growth early in the process is crucial, notes Varadarajan; an initial nonuniformity in nucleation can be propagated such that growth occurs preferentially in one location verus another. "We are avoiding the problem of nonuniform growth within a feature by dynamically controlling the voltage to a precise amount," he says. "Once the process is established and the growth front is happening, the additive concentration is influenced by how long the process has happened—that ends up taking over control, so microscopic control of the field is not so important." Thus, millisecond control is sufficient for the fill process.

Other features of the new system include the use of a proprietary low-corrosion electrolyte that the company says reduces the propensity for killer defects; and reducing the process edge exclusion to only 1mm, which increases the usable die area and thus the number of chips per wafer. Changes made to the wafer-holding apparatus that reduce the edge exclusion include a much lower profile, and the use of exotic materials to handle the strength requirements of the clamping, according to Varadarajan. He points out that Novellus' sealed contact technology excludes the backside and a frontside corner of the wafer from the electrolyte, so only the face of the wafer actually sees the liquid.

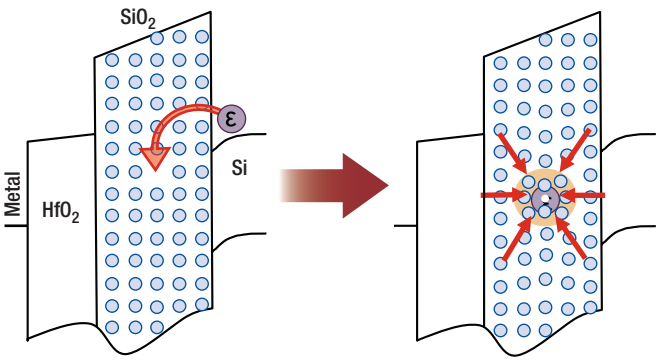
"Within this dry space, we have electrical contacts to pass the current," he says. Looking ahead to 16nm, Varadarajan explains that while there is no patterning capability to prove that 16nm can be achieved in a broad sense, from a damascene standpoint, the company believes that the smallest geometry that will probably be seen is on the order of 1.5× the node (varying among end-users) —e.g., for the 22nm node, aggressive features are on the order of 28nm, unlike the contacts which will be at design rule.

Thus, the company projects that its validated filling capabilities on extremely small trenches (22-23nm) are roughly the dimensions that will be seen on a 16nm logic device. "We believe the fill capabilities we designed into the system have some legs to carry us to a node beyond 22nm," Varadarajan predicts. ***—D.V.***

New transistor noise model helps ID defects in gate stacks

Researchers from SEMATECH have developed a new way to model transistor noise that can help extract defect characteristics from low-frequency noise data in advanced gate stack transistors with conventional and novel dielectrics, seen as a key step in defect analysis and elimination needed for device scaling.

Low-frequency noise—random fluctuations in device current, caused by electrons jumping back and forth from the substrate into a defect in the dielectric—is of increasing concern as CMOS is scaled ever further. Conventional modeling for such noise, based on "elastic tunneling," looks



Schematic representation of the electron trapping process: relaxation caused by the trapped charge involves displacements of the lattice atoms around the defect. The energy barrier associated with the motion of the atoms around the defect is responsible for slowing down the trapping/detrapping process, significantly increasing electronic capture and emission times. (Image courtesy of SEMATECH)

at the time of an injected electron capture by a bulk defect as controlled by the tunneling process. Unfortunately, this has been shown by NIST researchers to not work as predicted, and the SEMATECH researchers agree, saying the measured characteristic times are "several orders of magnitude longer than the estimates based on the tunneling times;" carrier capture rates can be off by a factor of 1000× or more.

The new work, reported at the IEEE's recent Integrated Reliability Workshop, instead turns to the concept of "lattice relaxation" around a defect—when a defect traps an electron, the neighboring nuclei "feel" it and shift positions (i.e., "relax") to accommodate the new force. This requires a certain amount of energy, which amounts to a barrier that slows the rate of charge capture, SEMATECH notes in a statement. "The times of capture and emission by the bulk oxide traps might be controlled to a great degree by the trap structural relaxation rather than by electron tunneling," the researchers note in their paper abstract.

Using their proposed methodology, the researchers say they were able to extract characteristics of defects in high-*k*/metal-gate (HK+MG) and SiON/poly-Si transistors, and in the tunnel oxide of the charge trapping memory devices (TANOS).

"To optimize noise performance in various applications, we need to be able to accurately simulate the processes responsible for noise," says Gennadi Bersuker, project manager of electrical characterization and reliability at SEMATECH, and one of the paper's authors, in a statement. "With the proposed model, the reliability community now has a means of identifying the atomic structure of the defects, allowing feedback to process and integration groups to facilitate reduction and elimination of the defects."

According to Michael Shur, professor at Rensselaer Polytechnic Institute, "The SEMATECH work explains several orders of magnitude difference between older, so-called, tunneling models and the noise measured in advanced CMOS with ultrathin oxide layers." — ***J.M.***

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IBM pushes AFM to image molecular structure

Researchers at IBM in Zurich, Switzerland, have captured the "anatomy" of a molecule using noncontact atomic-force microscopy (AFM), peering through the surrounding electron cloud to capture images "with unprecedented resolution."

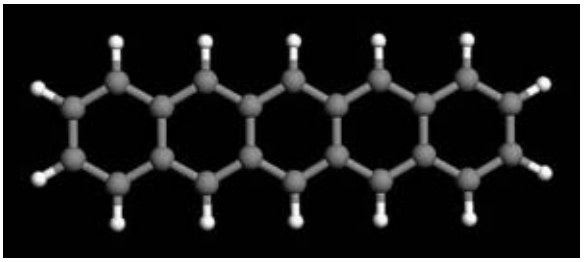

Figure 1. Ball-and-stick model of the pentacene molecule: five linearly fused hexagonal rings of benzene, comprised of 22 carbon atoms (inner gray balls) and to which are bound 14 hydrogen atoms (outer white balls). The entire molecule is 1.4nm in length; spacing between neighboring carbon atoms is 0.14nm. (Image courtesy of IBM Research/Zurich)

The method, a longtime goal of surface microscopy, involves an AFM operated in an ultrahigh vacuum at very low temperatures (-268°C), to image the chemical structure of individual pentacene molecules (1.4nm in length). Key was using an "atomically sharp" tip apex to measure the forces between the tip and sample. Also, picking up single atoms and molecules showed that the foremost tip atom/molecule governs the AFM contrast and resolution. Terminating the AFM tip with a carbon monoxide (CO) molecule was shown to yield optimum contrast at a height of ~0.5nm, notes IBM scientist Leo Gross, in a statement. Another key: deriving a complete 3D force map of the molecule, enabled by the AFM's mechanical and thermal stability.

Corroborating the results using first-principles density functional theory calculations, the researchers also figured out what caused the atomic contrast: Pauli repulsion between the CO and the pentacene molecule, explains IBM scientist Nikolaj Moll (referring to a quantum mechanical force that prevents two identical electrons from coming too close together). van der Waals and electrostatic forces, the scientists determined, "only add a diffuse attractive background."

The AFM's imagery, seen here compared to a diagram, is striking: hexagonal shapes of the five carbon rings and carbon atoms are clearly resolved, and hydrogen atoms also can be discerned. (IBM has posted more pictures on Flickr, and even a video on YouTube.)

Most significantly, says IBM, this atomic-scale imaging, combined with similar experiments earlier this summer that measured the charge state of single atoms, help better understand charge distribution at the atomic scale, pointing a way to create molecular-scale devices and networks.

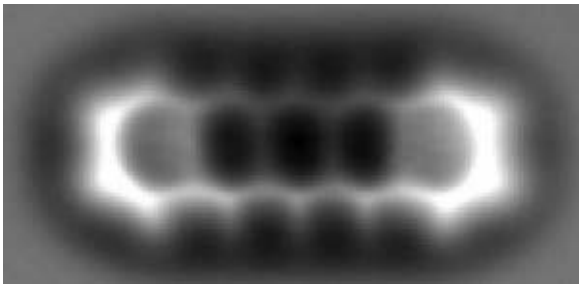

Figure 2. The inner structure of a pentacene molecule imaged with an atomic force microscope. Pixels correspond to actual data points. (Image courtesy of IBM Research/Zurich

The work was done in collaboration with Peter Liljeroth of Utrecht University, and published in the Aug. 28 issue of the journal *Science*. — ***J.M.***

Mentor tips plans for unified Si test, yield analysis

Mentor Graphics is launching what it calls a comprehensive test and yield analysis platform to help customers drill down through failure analysis data to better identify and fix defects, thus saving time and improving yields.

The plan combines Mentor's embedded compression and automatic test pattern generation (ATPG) technology with the built-in self-test (BIST) technology for memory and logic acquired with LogicVision in May 2009. The new product line, Tessent, incorporates a Diagnosis tool for automated scan test failure collection and diagnosis, and a new YieldInsight product to analyze/visualize and drill-down through large volumes of production test failure diagnosis data. Also included are silicon debug/characterization (LogicVision's SiliconInsight product) and layout-aware diagnosis (via Mentor's tools).

The Diagnosis software performs volume diagnosis of manufacturing test failures (based on FastScan or TestKompress scan patterns), providing information beyond single-device defect location to classify all major defect mechanisms, and uses layout information to identify physical features and cell types associated with a defect type (e.g., attributes ranging from via type to metal layer and failing scan cells). Diagnosis results are compared to expected distribution to help spot patterns in the failure diagnosis data that might point to systematic issues. Further analysis helps understand the impact of each systematic problem and select devices for physical failure analysis that clearly exhibit the identified problem.

As an example, the company described a customer performing signature analysis on failure diagnosis data indicated a systematic issue contributed to yield loss, further identified as a single defective via on Layer 5. A manufacturing process change was made to correct the issue and eliminate future yield excursions.

Going forward, Mentor's BIST offerings will be based on the former LogicVision platform, and test-pattern generation will be based on Mentor's TestKompress and FastScan platform; some of Mentor's former BIST products, and LogicVision's ATPG products, will be discontinued. Mentor said it will invest and develop mixed-signal BIST for Serdes and PLL testing as well as LogicVision's SiliconInsight line, and will seek to add more functionality to the Tessent line for "emerging challenges related to test." —***J.M.***

An analysis of potential 450mm CMP tool scaling questions

EXECUTIVE OVERVIEW Since the invention of the integrated circuit, microchips have been fabricated on progressively larger silicon wafers to take advantage of the economies that can be realized from being able to process more die simultaneously. In the early 1970s, a 50mm wafer could hold about fifty 0.5 x 0.5cm dice. More than 36 times as many die of the same size can now be processed on a 300mm wafer. Even allowing for the greater cost of the larger wafer and the tools needed to process it, the growth in wafer area has historically been a significant factor in reducing the cost per die. This article discusses the considerations that arise with respect to chemical mechanical planarization (CMP) for 450mm wafer manufacturing.

A change to 450mm would involve a significant investment in tools and fabrication facilities, so questions naturally arise about whether tools that are currently used for 300mm could, in some cases, simply be scaled up and whether there are any problems created by doing so.

For example, in CMP processes:

- Would rotary tool scaling to 450mm lead to dangerous heating of the pad or wafer?
- Would slurry costs become prohibitive due to the increase in pad area?
- Could the polishing pad still be conditioned in the same way?

We investigated many of these questions for an example CMP process run on a hypothetical 450mm rotary polisher. For comparison, identical simulations were also run for similarly configured 200mm and 300mm tools.

Araca, Inc., developed the specialized programs that were employed. The software implements many of the key physical models needed for tool-scale CMP studies. For example, we use a three-dimensional (3D) load and moment balance model to simulate rough surface contact between the wafer and retaining ring and the pad. This makes it possible to estimate the slurry film thickness distribution under the retaining ring and the wafer. Since slurry has a high capacity to absorb heat, this is important for getting the correct wafer and ring temperatures.

Leonard Borucki, **Ara Philipossian**, Araca Inc., Mesa, AZ USA; **Michael Goldstein**, Intel Corp., Santa Clara, CA USA

The software also has a model for the injection of slurry at multiple points onto plain (un-grooved) pads that have rough surface textures, and for the subsequent flow over the pad, under the retaining ring and wafer, and ultimately off of the platen. A 3D thermal model simulates frictional heat generation by the wafer and retaining ring, and the transport and transfer of heat throughout the tool by the slurry and by the rotation of the polishing head and the platen.

A schematic layout of the hypothetical rotary polisher is shown in **Fig. 1**. Both the platen and head rotate counterclockwise. Slurry is applied to the pad within the wafer track using a bar applicator with nozzles spaced 1" apart. As the wafer size is scaled up, the number of nozzles is correspondingly increased. The total flow is divided equally between the nozzles.

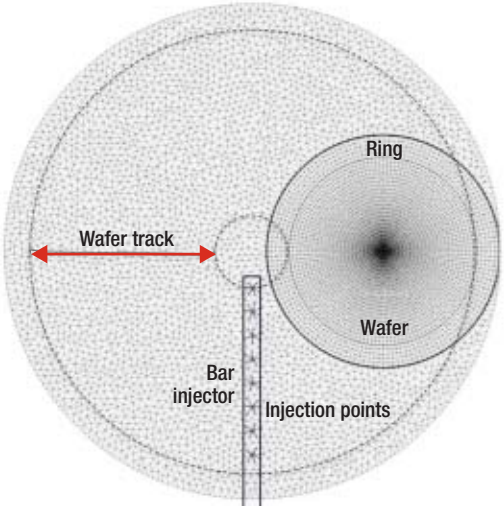

Figure 1. Rotary CMP tool schematic layout.

The slurry viscosity and thermal properties are typical for slurries in current use. For the pad, the mechanical, thermal, and surface textural properties correspond to a commonly used commercial hard pad with a soft sub-pad. The polishing head poses a special thermal analysis problem. Because the head design for 450mm is not known and, therefore, cannot be simulated in detail, we assume a simple head for all platform sizes consisting of a ½"-thick aluminum plate. A thin polymer wafer backing film is interposed between the wafer and the head. The retaining ring is assumed to be 1" wide regardless of wafer size, mechanically independent of the wafer, and to have the thermal properties of PEEK (polyetheretherketone).

Platform comparisons

To compare the platforms, we use the same polishing time (1 min.), the same wafer and ring pressures (2psi for the wafer, 4psi for the ring) and a constant pad/wafer relative sliding speed of 1m/sec. Constant pressure and sliding speed are a starting point for obtaining

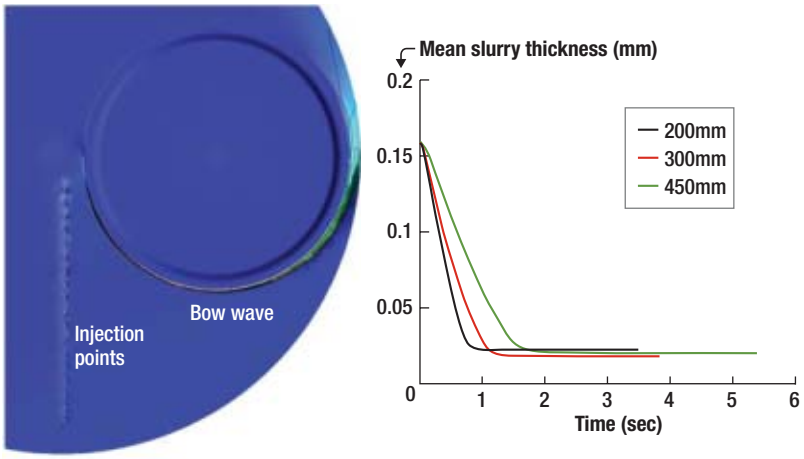

Figure 2. Slurry film top view (left) and mean film thickness comparison (right)..

the same material removal. For simplicity, we assume that the wafer and platen co-rotate so that the relative sliding speed is constant everywhere on the wafer.

On a rotary tool, the distance between the center of the wafer and the center of the platen must increase with the wafer diameter; therefore, a constant relative sliding speed implies that the platen rotation rate must decrease as the wafer size increases. Thus, at 1m/sec, the platen rotation rate is ~69rpm for 200mm, 47rpm for 300mm, and only 33rpm for 450mm.

What should the slurry flow rate be for a 450mm process? One idea would be to scale the slurry flow rate with the pad area. The proposed pad diameter for 450mm polishing is 1094mm, compared with 762mm for 300mm wafers and 508mm for 200mm wafers (some variations exist). Based on area, the slurry flow rate for a 450mm process should be about 2.1 times that of the same 300mm process and 4.6 times greater than a 200mm process. Scaled up in this way, a 200mm process consuming slurry at 150ml/min would require almost 700ml/min on a 450mm tool—a large increase.

There is a more subtle way, however, to analyze the question. Reducing the platen rotation rate has several effects, one of which is to reduce the slurry's outward centripetal acceleration. At a fixed distance from the platen center and at a fixed flow rate, reduced acceleration increases the slurry film thickness. For all tool sizes, however, the thickness of the gap between the wafer or ring and the pad is determined by the pad properties and applied pressures, and is, therefore, approximately constant. This suggests that one should try to scale the slurry flow rate so that the average slurry thickness on the pad outside of the ring and wafer also remains constant as the tool is scaled up.

A rigorous analysis is feasible when the slurry flow outside of the pressure ring is modeled using the thin film equation [1]—a simplification of the incompressible Navier-Stokes equations that is suitable for modeling transport over a pad surface without grooving. A mathematical scaling analysis of the thin film equation suggests that the slurry flow rate should be scaled like the ratio of the pad areas times the ratio of the rotation rates. This scaling procedure reduces the flow rate for 450mm to 700 x 33/69 = 334ml/min in the example, or about half of what area scaling indicates.

Figure 2 shows a top view of the steady state slurry film thickness on a 450mm tool. The bow wave is visible at the upstream side of the ring, and it is clear that the slurry thickness under the ring is smaller than the thickness under the wafer because of the applied pressure difference. The slurry thickness in the bow wave never exceeds 1mm. The graph in the same figure shows that the mean slurry thickness on the pad reaches steady state within a few platen rotations, and that the slurry flow rate scaling law has succeeded in producing nearly the same mean film thickness (~20μm) for all tool sizes.

Because the slurry used in a polishing process may be thermally activated, the temperature distribution of the wafer, or wafer body temperature, is of interest. The calculated steady state temperature rise above ambient for the surface of the pad, the ring, and wafer for a 450mm tool is shown in **Fig. 3** (pg. 13). The largest temperature increase—17°C—occurs on the retaining ring near the pad center where cooling by fresh slurry is minimal. The ring temperature is also affected by the coefficient of friction, which is larger for PEEK than for the wafer.

Figure 3 also shows a scatter graph of the temperature increase

continued on page 13

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CMP tool scaling continued from page 11

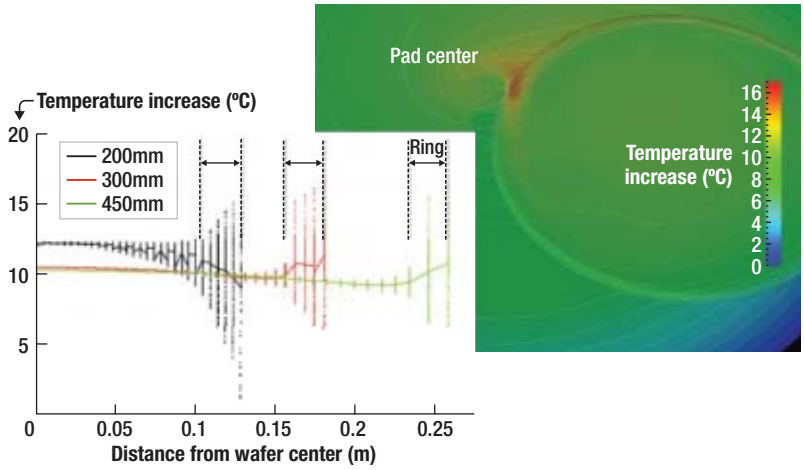

Figure 3. Wafer and ring radia ltemperatures (left) and a 3D-view (right) .

as a function of radius on the wafer and ring for the three tool sizes. The wafer is slightly center hot, a prediction that has been verified experimentally [2]. Surprisingly, the wafer temperature distribution for 450mm is predicted to be a smooth extension of the distribution for 300mm. At the edges of the wafer, there is a suggestion of wafer edge heating due to heat transfer from the ring; but again, it is the same for 450 and 300mm.

Another important quantity is the temperature rise of contacting pad summits, or the flash temperature increment [3]. Most of the heat in CMP is generated at the contact points between pad summits and the wafer or ring. Mechanically mediated material removal of chemical reaction products formed on the wafer also occurs at the contacts. Since the real contact area is often less than 0.1% of the wafer area [4], contacting pad summits are probably hotter than the wafer, and their temperature may, therefore, dominate the chemistry.

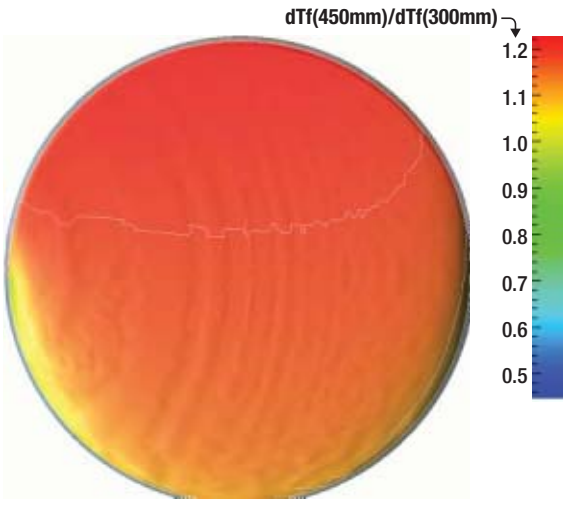

Figure 4. Ratio of the flash temperature increment for 450mm to that for 300mm.

Figure 4 shows the ratio of the flash temperature increase predicted for a 450mm tool to the prediction for a 300mm tool. Since summits spend more time in contact with the ring and wafer on a 450mm tool due to the lower platen rotation rate, the flash temperature increment for 450mm is expected to be 10-20% higher than for 300mm, with a 20% increase over the trailing one-third of the wafer. Theoretically, this could increase the chemical reaction rate by a potentially significant percentage, depending on the activation energy of the process, and significantly affect removal rate uniformity in the case of chemically limited CMP processes.

For most polishing processes, the pad surface must be continually renewed or conditioned to prevent the buildup of polishing debris and to counteract plastic deformation and abrasive wear, which can lead to a decrease in material removal rate. This is usually done with a diamond conditioning tool. If the conditioning procedure is directly transferred as the tool size increases, however, the rate at which the conditioner refreshes the pad surface will decrease in proportion to the pad area. Thus, the vertical pad cut rate for 450mm should be about 20% of the rate for 200mm if the conditioner load and sweep frequency are kept the same.

One solution—increasing the load on the conditioner by the area ratio—will decrease conditioner life by the same ratio. Furthermore, with a slower platen rotation rate and a fixed duration process, the conditioner will make fewer passes over each point on the pad, suggesting that the sweep frequency should also be increased to compensate. Deeper study of this issue is required to determine whether there is a viable solution.

Conclusion

Simulations suggest that if the polishing pressure, relative sliding speed, and mean slurry thickness are held constant when scaling to 450mm, then slurry consumption will increase moderately and the wafer and pad temperature will be essentially unchanged. Because it is necessary to decrease the platen rotation rate to keep the speed constant, it is predicted that there will be an increase in the flash temperature at contacting summits, which may affect uniformity in chemically sensitive processes. The most difficult problem, however, is how to condition a much larger pad within the fixed time allotted to each polishing step.■

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Biographies

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300mm Prime and the prospect for 450mm wafers

EXECUTIVE OVERVIEW For five decades, the semiconductor industry has been delivering continuous improvement in the performance of semiconductor devices while simultaneously reducing prices. The open market price for a million bits of DRAM memory and the price for a million instructions per second of microprocessor performance have both been reduced by an average of ~35% per year since they were introduced in 1970 [1]. Recently, the NAND Flash prices per million bits have been reduced at an even faster rate of ~64% per year [1]. For semiconductor companies to succeed or even survive in such an aggressive environment, rapid continuous improvement in costs is essential. This article discusses the cost savings that could be realized by the industry moving to 450mm wafer manufacturing.

The semiconductor industry has been able to deliver rapid price reductions by combining several factors to reduce costs:

- Yields were once low across much of the industry, but today routinely exceed 90% for even the most complex products within the first 12 months after their introduction to the market.
- Linewidth shrinks of 30% reduce die area by 50% and cost by ~40%. Whereas linewidth shrinks were once every three years, the last several generations have been on a two-year timeline, further accelerating cost reductions.
- Increases in wafer size, such as the 200mm to 300mm transition, increase wafer area by 2.25x and decrease costs by ~30%.
- Improvements in other factors, such as the operating efficiency of equipment, also contribute.

	Intel microprocessor	Samsung NAND Flash
300mm	$6.28	$2.39
450nm	$4.64	$1.69
Cost savings	26%	29%

Table 1. 2015 cost per square centimeter simulation results [6].

These four factors have, to date, been sufficient to maintain gross margins in the industry, but now and in the near future, some of these factors will show a reduced effect on cost reduction. Yields are now so high and reach such a high level so quickly that further improvement will have only minimal effect on cost reduction. This is not to say that yield isn't important; it is, but there is less room for future improvement. Linewidth reductions should continue on a two-year cycle for a few more generations, but will then begin to approach physical limits—slowing and eventually stopping.

Scotten W. Jones, IC Knowledge LLC, Georgetown, MA USA

There are also questions concerning the economics of future lithography solutions, such as extreme ultraviolet (EUV) needed to keep shrinking linewidth. Wafer size transitions have slowed, and many have openly questioned whether the industry will ever make the transition to 450mm wafers. It has been estimated that the semiconductor equipment industry spent $11.6 billion dollars developing 300mm tools [2]—an investment that it is still struggling to recoup. With 450mm tool development costs estimated to cost $25 billion [2] and most equipment companies losing money, reluctance to engage in another wafer size transition is easy to understand.

300mm Prime

300mm Prime is an ISMI initiative to improve efficiency of 300mm equipment and maintain historical cost reduction rates without resorting to a 450mm wafer transition. In 1995, SEMATECH studied the overall equipment effectiveness (OEE) of 350nm and larger linewidth equipment, and found that the equipment was producing good useable product only 30% of the time [3]. The remaining 70% of the time was lost to down time, no product or operator being available, speed, scrap, test wafers, set up, and other factors.

Even as late as 2003, SEMATECH still found OEE was only 40% [4]. Clearly, there is great opportunity for improvement in equipment productivity. This is, in fact, the key reason why 300mm equipment is designed to accommodate two-input FOUPs at once—as one FOUP is emptied, a second one is ready, and product is always available for processing. To date, 300mm Prime has made progress but has not been able to meet the goals outlined for the program of a 50% cycle time reduction and 30% cost reduction [5]. In fact, no one has yet been able to outline a path to reach the 300mm Prime goals, leaving the eventual need to transition to 450mm wafers on the table.

450mm considerations

For 450mm to ever become a reality, the industry needs to be convinced that 450mm wafers will, in fact, deliver a sufficient cost reduction to justify the development cost, and then some kind of

The 300mm Prime effort-to-date has failed to achieve the program goals of a 50% cycle time reduction and 30% cost reductions. Simulations suggest that 450mm manufacturing is able to at least deliver close to a 30% cost reduction. Additionally, as material costs come down with learning, 450mm cost savings should get better.

partnership will need to be established between semiconductor manufacturers and equipment companies to fund the development. IC Knowledge produces a widely used IC Cost Model in the industry [6], and here, we present some simulations of 450mm wafer costs that use our commercial tool to look at possible cost savings.

For this study, we have chosen to model Intel microprocessors and Samsung NAND Flash, and have modeled 22nm processing in a plant built in 2014. To calculate 450mm wafer processing costs relative to 300mm, we have to project equipment costs and throughput differences, as well as materials usage and cost trends. We have assumed 450mm equipment will have similar throughput to 300mm equipment and cost 1.3x times as much. This assumption is consistent with the 200mm to 300mm transition.

We have forecasted 450mm wafer costs based on an initially higher cost per square centimeter cost due to scrap issues that, over time, will slowly approach the cost per square centimeter cost seen for 300mm. This trend is consistent with the last several wafer size transitions (**Table 1,** page 14).

The results in **Table 1** suggest that 450mm delivers cost reductions are consistent with past wafer transitions and so would be beneficial to semiconductor manufacturers. Higher initial material costs for 450mm reduce cost saving in the first few years after the wafer size is introduced, so that in later years, cost savings would be even higher on a percentage basis.

The capital efficiency challenge

We estimate that the cost to build and equip a 300mm fab is only 60% of the cost of building and equipping a 200mm fab with the same die output. At the same time that 300mm was ramping up, the semiconductor industry was transitioning from ~15% per year revenue growth to the ~4% per year currently seen. We believe this represents a maturing of the industry and is likely to continue for the foreseeable future.

Combining lower semiconductor market growth with improved capital efficiency has resulted in a capital equipment market that we expect to be essentially flat from 2000 to at least 2015 [1]. If 450mm equipment delivers a capital efficiency improvement equivalent to 300mm tools, we are hard pressed to see how the equipment industry survives. This is an area that will have to be addressed for 450mm tools to be developed.

A couple of recently published articles on 450mm contain statements we disagree with and wanted to examine further:

In "Contemplating 450mm," Daren Dance and David Jimenez of Wright, Williams and Kelly Inc., present some of their own cost modeling and conclude that 450mm wafers will be more expensive per square centimeter than 300mm wafers [7]. The largest segment of their costs is depreciation, so we decided to examine that result more closely. Reading off of their graph, we get ~$4.20/cm^2 for depreciation at 300mm, and $6.50/cm^2 for 450mm. If you consider that there are 2.25 times as many cm^2 in a 450mm wafer, their projection implies that the 450mm tool set will be 3.5 times as expensive as a 300mm tool set. With an assumption such as that, of course, the cost goes up.

At 300mm, toolset costs averaged ~1.3 times the cost of equivalent 200mm tools. There has been some commentary suggesting that at 450mm, the cost multiple may be higher than 1.3x and that the throughput may be lower, but a 3.5x cost increase strikes us as extreme. We would also argue that the increases Dance and Jimenez project for maintenance, and the flat process materials cost per square centimeters, are also pessimistic.

In "What Are the Alternatives to 450mm Wafers?," Jason Ignizio makes the statement that if the increases in cycle time seen from 200mm to 300mm wafers is repeated at 450mm, cycle time efficiency will decline [8]. The increase in cycle time seen at 300mm is the direct result of a design decision made by the industry standards committee to design tools to accept multiple input cassettes maximizing utilization as discussed above. Multiple input cassettes basically ensures that no tool runs dry of wafers, but also increases the wafers waiting in queue driving up cycle time. Unless some other cycle time-utilization trade-off decision is made at 450mm to maximize utilization, then 450mm cycle time should not be intrinsically worse than 300mm cycle time (unless tool throughput is significantly lower).

Conclusion

The 300mm Prime effort to-date has failed to achieve the program goals of a 50% cycle time reduction and 30% cost reduction. Simulations suggest that 450mm manufacturing is able to at least deliver close to a 30% cost reduction. Additionally, as material costs come down with learning, 450mm cost savings should get better. ■

Biography

Scotten W. Jones received his Bachelors of Science from the U. of Rhode Island, and is a senior member of the IEEE, a member of the Electrochemical Society, and is president of IC Knowledge LLC, P.O. Box 20, Georgetown, MA 01833 USA; 978-352-7610; sjones@icknowledge.com; www.icknowledge.com.

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NEW MATERIALS

EUVL resist and materials development for the 22nm node and beyond

EXECUTIVE OVERVIEW Leading-edge semiconductor manufacturers have targeted 2011 for the pilot line introduction of extreme ultraviolet lithography (EUVL). This aggressive goal can be accomplished only if high power sources become available for both scanners and mask inspection tools. Equally important to the success of EUVL introduction are mask infrastructure and production-worthy resist/materials processes. Currently, consortia seem to have emerged as the preferred business model to facilitate EUV introduction. Because this model minimizes cost and risk, consortia may be the only organizations that can make EUV successful.

Photo 1. The Resist Outgassing Test Stand.

To enable the 32nm half-pitch (hp) node, the industry introduced multiple variations of 193nm immersion double patterning (193i DP). When the decision was made to reduce the critical dimension (CD) used to make the highest speed microchips to 32nm, it was obvious that EUV was not ready. The target node for EUV introduction has, therefore, been changed to 22nm. As resist materials have been driven to resolve 22nm features at places such as SEMATECH's Resist and Materials Development Center (RMDC), and the path to high power sources seems to be reasonably attainable, EUV insertion now appears a reality. Accordingly, SEMATECH's lithography group has organized itself to facilitate the rapid introduction of EUVL.

The Lithography Division

SEMATECH's Lithography Division comprises four technical focus groups:

- *EUV Lithography*—Ensure member companies have the infrastructure elements required to support pilot line introduction by 2011, address issues hindering high volume manufacturing (HVM) introduction, and support extendibility of EUVL.
- *Mask Strategy*—Ensure the availability of defect-free EUV masks by 2011 for 22nm hp by building infrastructure tooling for EUV mask and blanks.
- *Alternative Lithography*—Assess the feasibility of alternative lithographic technologies to meet ITRS specifications for 22nm hp, and provide testing facilities for member companies.
- *Resist and Materials Development Center*—Provide world-class exposure capability, and build the leading center for supplier resist and materials research to enable 22nm patterning technologies and beyond.

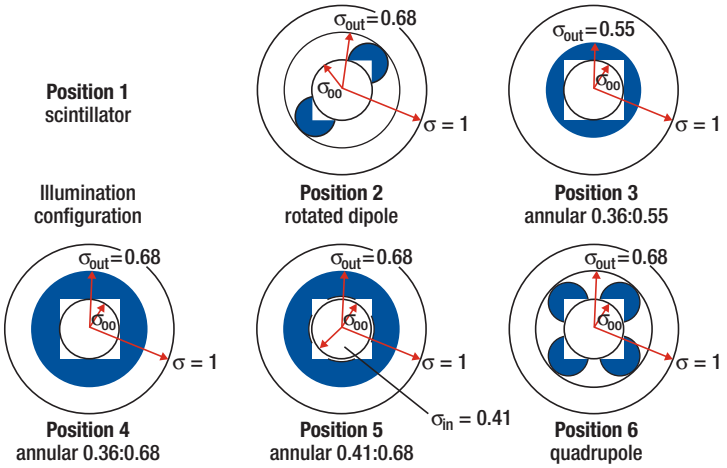

Figure 1. Dipole and quadrupole illumination capabilities.

This organizational structure, particularly the RMDC, makes SEMATECH uniquely positioned to address the challenges of introducing EUVL.

Focusing on photoresist, the RMDC houses all the EUV photon access available to SEMATECH and, by virtue of its collegiate partners, resist associate members, and engineering staff, serves as the technology hub for all lithographic materials development capability.

The RMDC is a vertically integrated organization containing the EUV ROX outgas testing tool (**Photo 1**); EUV exposure capability of the micro exposure tools (METs) at the College of NanoScale Science and Engineering (CNSE) in Albany, NY,

Warren Montgomery, CNSE assignee to SEMATECH;
Bryan Rice, Intel assignee to SEMATECH, Austin, TX USA

Photo 2. The SEMATECH 0.3 NA MET optic at Lawrence Berkeley National Laboratory's Advanced Light Source.

and Lawrence Berkeley National Lab (LBNL; **Photo 2**); and an ASM Lithography full-field 0.25 NA alpha demo tool (ADT) at CNSE.

The RMDC has a 24/7 staff and a wide range of lithography support equipment. Recent technological advances in both EUV and 193nm imaging have been presented at the 2009 International Symposium on Extreme Ultraviolet Lithography and at the 6th International Symposium on Immersion Lithography Extensions.

Imaging and outgas testing capability

CSNE at SUNY Albany has developed and built a state-of-the-art outgassing test stand. With this equipment, resists and materials are qualified before being used on the EUV exposure systems (**Photo 1**). Data obtained using this system has been reported [1, 2].

The Albany Exitech MET (eMET), the Berkeley MET, and the 0.25 NA ADT provide imaging support to SEMATECH member companies and research partners. The eMET, which is ideally suited for contrast curve generation, was originally conceived as a screening tool to allow resist manufacturers to do a coarse screen on a large quantity of samples. Today, it can easily accomplish a coarse screen of five or more samples, allowing the best candidates to be tested for maximum resolution on the LBNL MET. This system is capable of imaging in the 22nm range and lower.

Once the best candidates in terms of resolution, linewidth roughness (LWR), and photospeed have been identified, the materials are typically tested on the full field ADT. RMDC staff handles all the imaging and wafer processing, and may also analyze and provide the data to RMDC users. A typical user will receive outgassing results, contrast curve information, process window data, ultimate resolution, critical dimension uniformity (CDU), and LWR.

This year, more than 2000 wafers have been exposed on the eMET tool. Since an upgrade in January, the eMET has been delivering 90% availability (24/7). This performance has allowed the characterization of hundreds of resist and underlayer samples. Upgrades have also improved resolution. For example, illumination options were increased, thus allowing dipole and quadrupole illumination capability (**Fig. 1,** pg. 16). The eMET can now image 24nm routinely and shows modulation at 22nm (**Fig. 2,** pg. 18); future planned upgrades will drive resolution to sub-20nm levels.

Integrated resist development

Another important component of the RMDC is the university-based materials programs focused on the design and development of novel imaging materials. Photoresist manufacturers participate in materials development on college campuses worldwide, working side by side with their competitors to resolve precompetitive materials problems. The results of this collaboration are well documented and have yielded several conference papers and promising new photoresist formulations.

The group at Cornell recently presented a paper, "Tethered naphthalene derivatives as sensitizers for sequential two photon photoacid generators for double exposure photolithography" [3], at the 6th International Symposium on Immersion Lithography Extensions. This work is leveraging Cornell's synthesis capability and SEMATECH's engineering/processing experience to drive the development of a less expensive double imaging approach.

SEMATECH has also published results of its efforts in key EUV resist problem areas. In collaboration with CNSE, underlayers of a given resist were optimized, and specifically designed

EUVL resist continued from page 17

physical properties were investigated that can help improve the overall performance of thin resists [4]. A joint SEMATECH/TOK presentation addressed the need for resist suppliers to develop test methodologies to predict the lithographic performance of their resist product, even though they do not have in-house EUV systems. The paper looked at photospeed testing of resist samples exposed using e-beam, DUV, and EUV to determine any possible correlation among the exposure regimes.

The ability to predict lot-to-lot dose and process window performance is a key deliverable from the photoresist manufacturer to the resist user. Determining whether photospeed testing is accurate is, therefore, critical for resist suppliers and users alike [4].

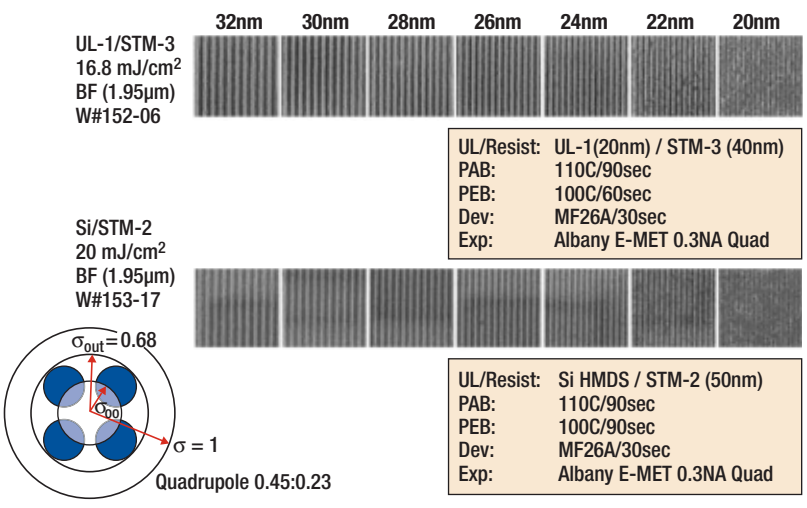

Figure 2. The eMET imaging at 24nm with modulation at 22nm.

To work with the photoresist and lithography development community, SEMATECH has started a Resist Associate Membership Program, through which photoresist developers, BARC makers, and other ancillary material manufacturers can gain access to SEMATECH's technical expertise and tooling capability to facilitate materials development while fostering an atmosphere of cooperation with member companies. The Associate Member Program currently has two charter members that are powerhouses in the photoresist industry: TOK and Shin Etsu. Discussions are in progress with other suppliers to expand this number by the end of 2009. The synergies that can form as a result of these alliances cannot be quantified.

Conclusion

The Resist and Materials Development Center has accomplished several key milestones, among the most notable the addition of two new industry partners: Shin Etsu and TOK. Additionally, driving the resolution of the Albany MET exposure system to 22nm while delivering more than 100 hours of weekly imaging access has enabled the optimization of hundreds of photoresist samples. A number of high-resolution EUV resists have also been characterized lithographically and tested on the EUV outgassing system. The learning from this testing has enabled resist outgassing specifications to be relaxed, thus allowing more resist to be tested using the ADT.

Finally, the etch resistance of resist formulations for 193nm applications has been improved, providing an opportunity to decrease layer-specific film thickness requirements. New, thinner resists will facilitate even higher resolution and a wider focus window for future process technologies. As the RMDC begins to integrate its resist formulations, outgassing results, and etch findings, more contributions to the industry can be expected. ■

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4. 6th International Symposium on Immersion Lithography Extensions, Oct. 18-21, 2009, Prague, Czech Republic.

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COAT/DEVELOP/BAKE

Defect reduction using POU filtration in a new coater/developer

EXECUTIVE OVERVIEW The fundamentals of microbridge defect reduction are not yet completely understood. Previously, it was concluded that microbridge precursors adsorb onto polar moieties within Nylon 6,6, by comparing defect density among polar filters (Nylon 6,6) and non-polar filters (HDPE and PTFE) [1]. The study presented here works toward a greater understanding of the adsorptive filtration-defect reduction relationship by additionally considering the effects of resist solvent polarity. The study also demonstrates how defectivity improvements via enhanced point-of-use (POU) resist filtration can be reproduced on next-generation process equipment [2].

The impact of pore size and membrane material polarity on the effectiveness of point-of-use (POU) filtration has been evaluated. Decreased pore size and increased polarity in membrane materials were confirmed to positively influence the effectiveness of microbridge defect removal by a POU filter in the LITHIUS Pro coater/developer system. Comparative analysis of different solvent systems validates a model of competitive adsorption whereby more-hydrophilic solvents and gel-like agglomerates preferentially interact with the Nylon 6,6 membrane surface. This suggests that adsorption is the dominant mechanism for microbridge defect removal via filtration. Therefore, utilizing filtration products built around polar membrane materials (like hydrophilic Nylon 6,6) will result in greater microbridge defect reduction than solely reducing filter pore size.

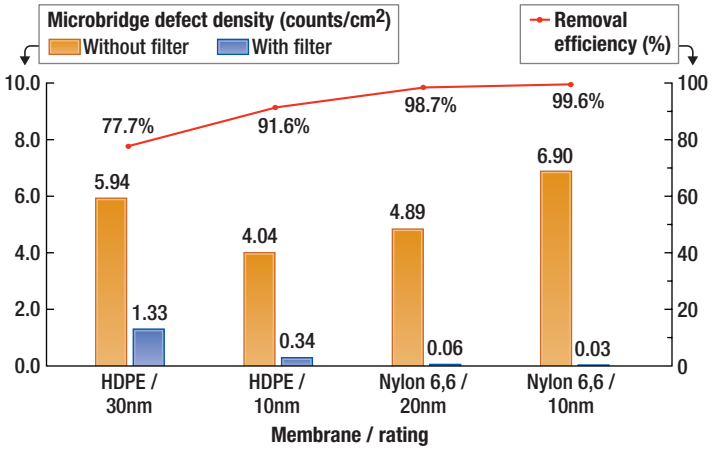

Figure 1. Microbridge defect reduction in TEL Lithius Pro using various point-of-use filters.

As lithographic pattern CDs continue to shrink, so does the tolerance for the size of photoresist defects, such as agglomerated microbridge precursors [3]. Microbridge defects are particularly observed in acrylate-based 193nm photoresists [1]. A Tokyo Electron CLEAN TRACK ACT 8 coater/developer system with 200mm wafers was used to demonstrate that POU filtration is effective to reduce microbridge defects, where pore size, membrane polarity, and surface modification were proven to be dominant factors [4,5]. To meet manufacturing requirements, Tokyo Electron developed a CLEAN TRACK LITHIUS Pro coater/developer system that can process 300mm wafers. In this study, the impacts of pore size and membrane material polarity on the effectiveness of POU filtration are evaluated.

The fundamentals of microbridge defect reduction are not yet completely understood. Previously, it was concluded that microbridge precursors adsorb onto polar moieties within Nylon 6,6, by comparing defect density among polar filters (Nylon 6,6) and non-polar filters (HDPE and PTFE) [1]. The present study works toward a greater understanding of the adsorptive filtration-defect reduction relationship by additionally considering the effects of resist solvent polarity.

Test methods

Effects of membrane polarity and pore size at POU. A standard 193nm resist was dispensed through various point-of-use filters, and was spin-coated onto silicon (Si) wafers using the coater/developer. To study the effect of membrane polarity, Nylon 6,6 and HDPE were used as polar and non-polar filters, respectively. The finest (10nm for Nylon 6,6 and HDPE) and next-finest (20nm for Nylon 6,6, 30nm for HDPE) available removal ratings that were commercially available for each filter type were used in a standard patterning process.

A 90nm half-pitch line/space pattern was printed using a 193nm (dry) exposure tool. After pattern development, defects were quantified using a KLA-Tencor 2360 inspection system. Microbridge defects were then identified using a scanning electron microscope (SEM).

Filtration of microbridge defect precursors in Fe-spiked resist. Microbridge defects do not have a regular morphology, but are likely composed of a gel-like substance. Metal contamination in photoresist increases defectivity by cross-linking acrylate polymer molecules and forming low-molecular-weight gel aggregates [6]. We

Toru Umeda, **Shuichi Tsuzuki**, **Toru Numaguchi**, Pall Corp. Inashiki-gun, Ibaraki-ken, Japan

POU filtration *continued from page 19*

attempted to create gel aggregates by spiking iron (100ppb, as Fe^{3+}, in diluted nitric acid) into a photo-resist polymer + solvent (propylene glycol monomethyl ether acetate [PGMEA]/Ethyl lactate mixture) solution, which was then aged up to 48 hours. Spiked resist of various aging terms were used to challenge 20nm rated Nylon 6,6 filters. Fe concentrations in both the influent and the effluent were measured using inductively coupled plasma-mass spectrometry (ICP-MS). The amount of Fe removed is assumed to correlate to the removal efficiency of gel-like microbridge precursors.

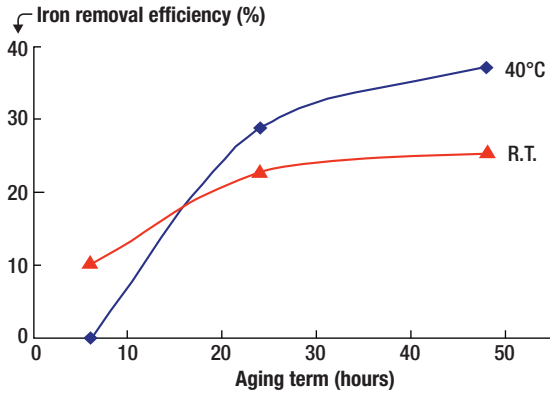

Figure 2. Fe removal efficiency of Nylon 6,6, filter vs. aging term of spiked resist.

Filtration of microbridge precursors within solvents of varying polarity. Three different solvent systems were evaluated: PGMEA/Ethyl lactate, PGMEA/PGMEA, and PGMEA/Cyclohexanone (each in a mixture). For nuclei metals, we spiked magnesium (Mg), nickel (Ni), and cadmium (Cd) (in diluted nitric acid) into each polymer + solvent system to follow a result of a study that these metals form remarkably greater concentrations of aggregate gels than Fe. The concentration of each spiking metal was 10ppb.

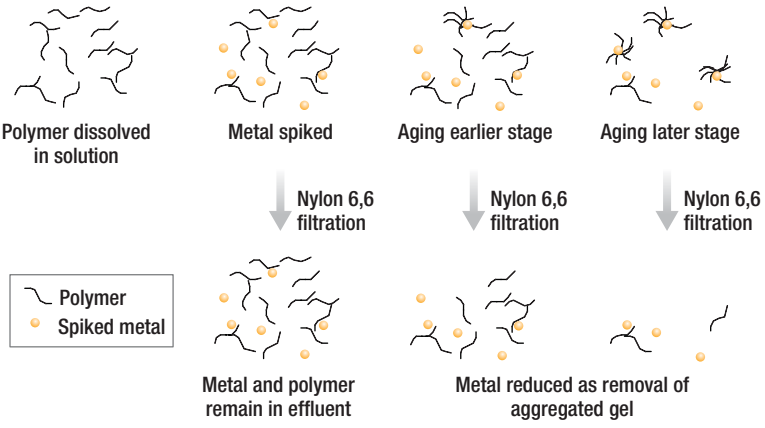

Figure 3. Interpretation model of the results shown in Fig. 2.

As with Fe-spiked resist, prepared solutions were used to challenge 20nm rated Nylon 6,6 filters. Metal concentrations in both the influent and the effluent were measured using ICP-MS. Again, the amount of removed metal amount is assumed to correlate to the concentration of gel-like microbridge precursors.

Results and discussion

Effects of membrane polarity and pore size. Figure 1 (pg. 19) shows the results of POU filtration in the coater/developer on microbridge defect density. The left y-axis corresponds to microbridge defect density (bar graphs). The right y-axis, "Removal efficiency," is the ratio of microbridge defect density values "with filter" to "without filter."

In the results, Nylon 6,6 filters showed better microbridge defect removal efficiency (ranging from 98.7 to 99.6%) compared to HDPE filters (77.7 to 91.6% reduction). In HDPE filters, microbridge defect removal efficiency was improved from 77.7 to 91.6% by reducing pore size from 30 to 10nm. In Nylon 6,6 filters, the measured defect density was too small to discern any difference between 20 and 10nm pores.

Results showing enhanced microbridge defect removal via decreased pore size and increased membrane polarity in POU filters have been reproduced within a next-generation coater/developer system.

Microbridge precursor reduction

Filtration of microbridge defect precursors in Fe-spiked resist. Figure 2 shows the iron removal efficiency of Nylon 6,6 filters in Fe-spiked resist that is aged to various extents. The removal efficiency of Nylon 6,6 filters appeared to increase with aging time. An interpretation of this result is illustrated in **Fig. 3**. Fe is introduced (spiked) into the resist solution in an ionic state. As time elapses, Fe ions serve as nucleation sites and begin to coordinate with aggregates of cross-linked acrylate gels. With additional aging, a greater amount of Fe ions becomes complexed with gel defect precursors. Given the demonstrated ability of polar Nylon 6,6, membrane to remove aggregated gel contaminants, it follows that a greater amount of Fe will be removed with resist aging time. Even after 48 hours of aging, however, the Nylon 6,6 filter does not completely remove all of the Fe. This is because all of the Fe has not complexed with aggregate gels.

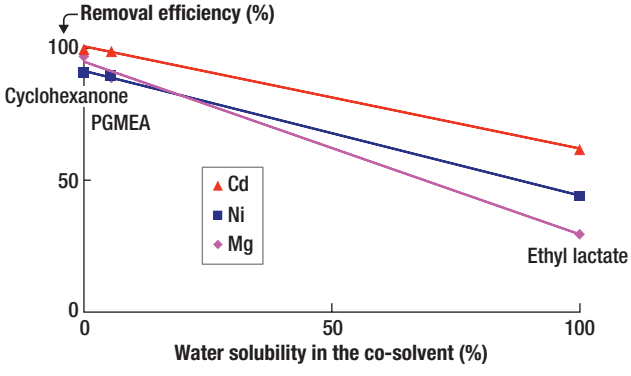

Figure 4. Water solubility in the solvent vs. metal removal efficiency in Nylon 6,6 filtration.

Filtration of microbridge precursors within solvents of varying polarity. It is known that solvent molecules compete with solute molecules for available adsorption sites on a solid surface [7]. The interpretation of the aging result suggested that the gel-like aggregates were polar in nature, and thus, hydrophilic. To study this hypothesis, the effect of solvent polarity (hydrophilicity) within a spiked resist on metal removal efficiency was evaluated.

Filtration results are given in **Fig. 4**. An inverse relationship is observed between metal removal efficiency and solvent hydrophilicity. In correlation with earlier results on Fe-spiked resist, a schematic

model used to interpret this observation is given in **Fig. 5**. In hydrophobic solvent systems, a greater number of adsorption sites on the Nylon 6,6 surface will be available to retain gel aggregates. Conversely, if the solvent is hydrophilic, the polar Nylon 6,6 adsorption sites are partly covered by solvent molecules and may have some effect on gel adsorption to the membrane surface. This suggests that competitive adsorption between gel aggregates and more-hydrophilic solvents can affect microbridge defect removal filtration. These results further validate surface adsorption as the dominant mechanism for microbridge defect removal via filtration.

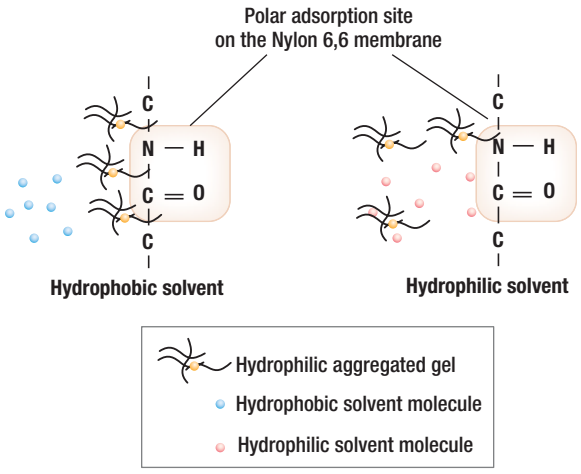

Figure 5. Schematic of competitive adsorption between hydrophilic aggregated gel and solvent molecules.

Conclusion

Decreased pore size and increased polarity in membrane materials were confirmed to positively influence the effectiveness of microbridge defect removal by a POU filter in the LITHIUS Pro coater/developer system. Also, comparative analysis of different solvent systems supports a model of competitive adsorption onto the Nylon 6,6 membrane surface between more-hydrophilic solvents and gel-like agglomerates. Results further validate membrane surface adsorption via polar (electrostatic) interactions as the dominant mechanism for microbridge defect removal via filtration. With an increased understanding of contaminant-surface interactions, it is clear that filtration products built around hydrophilic Nylon 6,6 membranes will continue to be a strategic component within next-generation litho process equipment to drive enhanced fluid cleanliness, defect reduction, and increased product yield. ■

Acknowledgments

The authors thank Tokyo Electron Kyushu Ltd. for providing POU filter evaluation data on microbridge defect reduction in the TEL Lithius Pro coater/developer system. The authors also thank JSR Corporation for providing test solution used in the investigation of the fundamentals of microbridge reduction. CLEAN TRACK ACT and LITHIUS Pro are trademarks of Tokyo Electron Limited.

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PRODUCT NEWS

Simultaneous FBE, DUV advanced film characterization

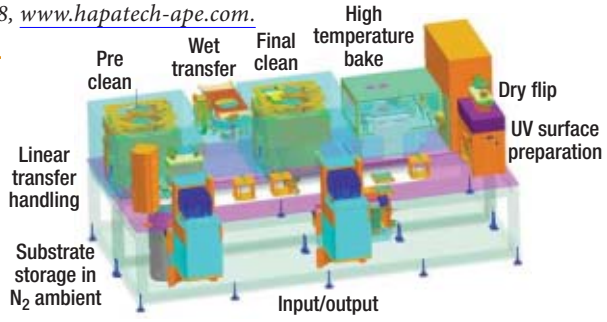
The S3000S metrology system ofers simultaneous measurement with multi-wavelength, multi-angle focus beam ellipsometry (FBE), and deep ultraviolet (DUV) reflectometry for in-line process control of advanced diffusion and fab-wide thin film applications. High-intensity, long-life laser light sources are designed to provide superior stability. A small beam size enables measurements in small test sites. An optional MAControl module provides one-step, uniform, non-destructive removal of the molecular airborne contamination layer on thin films to allow more accurate thickness measurement. **Rudolph Technologies**, *Flanders, NJ; 973/691-1300, www.rudolphtech.com.*

450mm metrology stage

This 450mm R/Theta/Z polar coordinate stage consisting of a linear, rotary, and Z axis offers a compact footprint for inspecting 450mm wafers. A bridge configuration provides a stable platform for mounting a variety of metrology systems. Additional features include a built-in prealigner, independent load-unload stations, a low-contact vacuum chuck (1.7% of a 450mm wafer), and an option for a lift pin mechanism for measuring wafer bow. **Micro Precision Automation**, *Richmond, CA; 510/215-0500, www.microprecisionautomation.com.*

Photomask system for 193i-DP, EUV, NIL

The MaskTrack Pro photomask processing system supports next-generation lithography processes for the 22nm half-pitch node—193 immersion/double patterning, EUV, and nanoimprint—with particle removal down to 20nm while protecting 100% of the mask structures and materials. A combination of physical and chemical cleaning technologies enables effective removal of organic/inorganic contamination without damaging features and material structures of the reticle. "Focused Spot Cleaning" is designed to precisely remove particles in defined areas of the mask, saving time after repair and eliminating overlay issues caused by backside contamination. A new design allows clustering of metrology systems and pod-in-pod stocking. **HamaTech Advanced Process Equipment**, *Sternenfels, Germany; ph: 49/0-7045-41-8, www.hapatech-ape.com.*



VOC oxidizer for PV manufacturing

The patent-pending VOC Thermal Oxidizer is designed to destroy more than 99% of volatile organic compounds (VOCs) from gases exhausted during the drying of photovoltaic metallization pastes in solar cell manufacturing, replacing remote abatement and VOC condenser options. The system mounts directly to the furnace to eliminate risk of solvent condensation; oxidizers at the entrance and exit of the dryer section are designed to achieve more effective abatement with faster belt speeds. **Despatch Industries**, *Minneapolis, MN; 888/337-7282, www.despatch.com.*

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detection system for both metals and dielectrics; a new wafer carrier, pad conditioner, and integrated post CMP cleaning. **Strasbaugh**, *San Luis Obispo, CA; 805/782-5383, www.strasbaugh.com.*

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INDUSTRY FORUM

Taiwan DRAM consolidation: Where's the money coming from?

Rupert Hammond-Chambers,
US-Taiwan Business Council, Arlington, VA USA

Cabinet reshuffles are common in Taiwan, and the recent cabinet turnover should be viewed in the context of a chastened President Ma Ying-jeou, whose poor handling of relief operations after typhoon Morakot warranted a fresh set of faces at the top. His plummeting popularity has undermined his broader agenda—rapprochement with China and the prospect of inking a cross-Strait free trade agreement.

Ma's new cabinet has been filled predominantly with conservative technocrats and academics. This was evident when new Minister of Economic Affairs' Shih, in his opening press conference, reiterated support for the Taiwan Memory Company (TMC) and consolidation of Taiwan's DRAM sector.

The Taiwan government is placing great stock in TMC and its partner, Elpida, as a consolidation vehicle, and in creating a company with the economies of scale to better weather cyclical downturns and to take on the Koreans. TMC submitted an application this fall to tap new government funds, which the Legislative Yuan then rejected over disagreement as to the return on investment for Taiwan's taxpayers, further exacerbating the government's vision for capitalizing this effort. If such funds would have been approved, they would have assisted in launching operations, and would have provided equity for investments in vulnerable legacy businesses, such as Powerchip. Companies that already use Elpida technology make logical acquisition targets for TMC, and are less attractive to such groups as Nanya/Inotera, who use Micron technology.

The government has clearly taken a somewhat ad hoc approach to its plan for TMC, and challenges remain unaddressed.

The first is the US$12 billion debt owed by the DRAM industry to Taiwan's state-owned banks. With the economic downturn and a drop in chip demand, coupled with serious overcapacity problems, this looming debt will come to a head at the end of the year. Businesses such as Powerchip and PROMOS will be grappling with repayment or finding new creditors in a highly challenging credit market.

Taipei's macroeconomic financial situation is also not good. The government is already scheduled to borrow a record amount to cover next year's budget shortfall. The situation has been further exacerbated by typhoon Morakot reconstruction funding.

There appears to be a presumption within the government that the TMC initiative will not meet any industry competition for acquisitions of distressed assets and other opportunities. Yet the Micron alliance that includes Nanya and Inotera is in a strong position to compete for assets and customers, challenging the government's ability to control the process. Nanya owner Formosa Plastics has deep pockets and strong government connections, well able to fend off even a government backed start-up such as TMC; and, Micron's technology is some of the world's most advanced.

Taipei's plans can receive a boost if DRAM prices hold steady, keeping production profitable. Cyclical demand and the introduction of Windows 7 should help sales. That said, the medium to long term picture is highly conditional on a return to sustained growth from the G3 economies and China, and there is simply no guarantee that will take place.

In addition, if global economic expansion starts to take hold, there will be strong pressure on the DRAM companies to fire up their currently mothballed production lines. That could easily pitch the DRAM price below the profitability mark, and the industry's challenges would remain acute and unaddressed.

It seems likely that, in the end, TMC and Elpida will manage to acquire and/or merge with PROMOS, Powerchip, and Rexchip to form one major Taiwan player built on Elpida's technology. Micron, Nanya, Inotera and Winbond could make up the second and competing group.

Finally, recent U.S. government interest in the funding mechanisms being employed by the Japanese and Taiwanese governments through Elpida and TMC adds further pressure to an unsteady process.

But the Taiwan government faces real challenges in raising the capital for this consolidation effort, and it will expect the DRAM debt to be repaid to its state-owned banks. This leaves a huge hole in the plan, with little clarity at this time from the Ma government about how all of these goals will be paid for. ■

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